IN THE CLAIMS

1. (currently amended) A method of making a microelectronic assembly, comprising:

providing a plurality of microelectronic elements;

~~connecting~~ adhering a dielectric layer to said plurality of microelectronic elements;

separating a portion of said dielectric layer from a remaining portion of said dielectric layer along at least one line extending between two of said plurality of microelectronic elements; and

removing the separated portion of said dielectric layer and at least one of said plurality of microelectronic elements ~~connected~~ adhered to said separated portion of said dielectric layer.

2. (original) The method of claim 1, wherein the plurality of microelectronic elements are connected to one another in a semiconductor wafer and the step of separating a portion of said dielectric layer includes dicing said wafer along the at least one line extending between two of said plurality of microelectronic elements.

3. (currently amended) The method of claim 1, wherein the ~~connecting~~ adhering step includes providing said dielectric layer having a first major face, a second major face, a first protective film over the first major face, and a second protective film over the second major face.

4. (currently amended) The method of claim 3, further comprising providing a first adhesive on the first major face of said dielectric layer, wherein the ~~connecting~~ adhering step comprises removing the first protective liner for exposing the first adhesive and ~~adhering the dielectric layer to the~~abutting the first major face of said dielectric layer against said plurality of microelectronic elements.

5. (original) The method of claim 1, wherein the

connecting step further comprises applying a flowable material to the plurality of microelectronic elements and at least partially curing the flowable material.

6. (original) The method of claim 1, wherein said plurality of microelectronic elements are selected from the group consisting of semiconductor chips, printed circuit boards, memory devices, interposers, stacked chip assemblies, semiconductor wafers and support layers.

7. (currently amended) The method of claim 1, wherein said plurality of microelectronic elements are integrated onto a wafer and wherein the separating step includes dicing the wafer for separating each microelectronic element into an individual unit having a portion of ~~the~~ said dielectric layer connected thereto.

8. (original) The method of claim 1, wherein the step of removing includes engaging one of the microelectronic elements with a pick and place machine.

9. (original) The method of claim 1, further comprising assembling the separated portion of said dielectric layer and the at least one of said plurality of microelectronic elements connected thereto with a microelectronic component.

10. (currently amended) The method of claim 9, further comprising applying adhesive to ~~the~~ said dielectric layer and adhering the separated portion of said dielectric layer to the microelectronic component.

11. (original) The method of claim 9, wherein the assembling step comprises adhering the separated portion of said dielectric layer with the microelectronic component.

12. (original) The method of claim 11, wherein the microelectronic component has a top layer and a plurality of

terminals exposed at the top layer.

13. (original) The method as claimed in claim 12, wherein the top layer of said microelectronic component includes a dielectric material.

14. (original) The method of claim 4, wherein the providing an adhesive on the first major face of said dielectric layer includes applying a flowable material to the plurality of microelectronic elements and partially curing the flowable material so that a layer of a partially cured, adhesive material is disposed on an outer surface of said dielectric layer.

15. (original) A method of making a microelectronic assembly comprising:

providing a dielectric layer including a first major face comprising a first adhesive, a second major face comprising a second adhesive, and a protective liner over the second adhesive;

juxtaposing a plurality of microelectronic elements with the first major face of said dielectric layer;

assembling said microelectronic elements with said dielectric layer by abutting said microelectronic elements against the first adhesive of said dielectric layer;

at least partially severing said dielectric layer while maintaining the protective liner as a single piece of material so as to form a plurality of individual microelectronic units overlying said protective liner, wherein each said individual microelectronic unit includes at least one of said microelectronic elements attached to an at least partially severed portion of said dielectric layer.

16. (original) The method as claimed in claim 15, further comprising:

providing the protective liner over the second adhesive and providing another protective liner over the first adhesive; and

removing the another protective liner over the first adhesive before the assembling step.

17. (original) The method as claimed in claim 15, wherein said dielectric layer comprises:

a fully cured inner region;

partially cured outer regions including the first and second adhesives at the first and second major faces of said dielectric layer.

18. (original) The method as claimed in claim 15, wherein the at least partially severing step comprises completely severing said dielectric layer while maintaining said protective liner as a single piece of material.

19. (original) The method as claimed in claim 15, wherein the assembling a plurality of microelectronic elements step comprises:

providing a semiconductor wafer; and

abutting said semiconductor wafer against the first adhesive material at the first major face of said dielectric layer.

20. (original) The method as claimed in claim 19, wherein the at least partially severing step includes dicing said semiconductor wafer to separate said microelectronic elements from one another.

21. (original) The method as claimed in claim 19, further comprising:

removing one of said individual units from attachment with said protective layer so as to expose said second adhesive material at the second major face of said dielectric layer;

abutting said second adhesive material with a second microelectronic element so as to form a microelectronic package.

22. (original) A method of making a microelectronic

assembly comprising:

providing a dielectric layer including a first major face comprising a first adhesive, a second major face comprising a second adhesive, and a protective liner over the second adhesive;

juxtaposing a semiconductor wafer including a plurality of semiconductor chips with the first major face of said dielectric layer;

assembling said wafer with said dielectric layer by abutting said wafer against the first adhesive of said dielectric layer;

maintaining the protective liner as a single piece of material while dicing said wafer and at least partially severing said dielectric layer for forming a plurality of individual microelectronic units overlying said protective liner, wherein each said individual microelectronic unit includes at least one of said microelectronic chips attached to an at least partially severed portion of said dielectric layer.

23. (original) The method as claimed in claim 22, wherein the at least partially severing step comprises completely severing said dielectric layer while maintaining said protective liner as a single piece of material.

24. (original) The method as claimed in claim 22, further comprising:

removing one of said individual microelectronic units from attachment with said protective layer so as to expose the second adhesive material at the second major face of said dielectric layer;

abutting said second adhesive material of said dielectric layer with a second microelectronic element for forming a microelectronic package.